REMARKS

Claims 1-4, 6-11, 13 and 14 were examined and reported in the Office Action. Claims 1-4, 6-11, 13 and 14 are rejected. Claims 1, 8 and 14 are amended. Claims 6 and 13 are canceled. Claims 1-4, 7-11 and 14 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. §103

A. It is asserted in the Office Action that claims 1-4, 6, 8, 10-11 and 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Patent No. 6,789,138 issued to Yoshizawa ("Yoshizawa ") in view of U. S. Patent No. 6,742,076 issued to Wang et al ("Wang"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2142

> [t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re

Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 1 contains the limitations of

> a universal serial bus (USB) host controller capable of coupling a plurality of queue heads to a frame list, wherein the plurality of queue heads are directly coupled to the frame list during initialization before coupling any split-isochronous transaction descriptors to the plurality of queue heads where split-isochronous transaction descriptors are supported.

Applicant's amended claim 8 contains the limitations of

> a first universal serial bus (USB) host controller and a second USB host controller, said first host controller capable of coupling a plurality of queue heads to a frame list, and a device coupled to said first and second host controllers, wherein the plurality of queue heads are directly coupled to the frame list during initialization before coupling any split-isochronous transaction descriptors to the plurality of queue heads where split-isochronous transaction descriptors are supported.

Applicant's USB host controller directly couples the queue heads during initialization before split-isochronous transaction descriptors are coupled to the queue heads. This prevents the queue heads from being subject to period promotion. Applicant notes that the terms USB host controller, and the USB data structures (queue heads, frame list, and split-isochronous transaction descriptors) are well known to those of ordinary skill in the art of USB technology. MPEP section 2111.01 asserts "'plain meaning' refers to the ordinary and customary meaning given to the term by those of ordinary skill in the art."

Applicant submits the *Enhanced Host Controller Interface Specification for Universal Serial Bus*, March 12, 2002, revision 1.0 ("EHCI Specification") to assist in understanding the prior art and also for the plain meaning of the above-mentioned data structures, as used by Applicant. Applicant asserts that section 3 Data Structures of the EHCI Specification defines the above-mentioned data structures. In particular, section 3.1 of

the EHCI Specification defines the frame list; section 3.4 of the EHCI Specification defines the split transaction isochronous transfer descriptor; and section 3.6 of the EHCI Specification defines the queue head. Standard USB 2.0 operation involves attaching isochronous transaction descriptors directly to the frame list (See Applicant's Fig. 5; Fig 4-8 on page 67 of the EHCI Specification). Applicant's claimed invention changes the standard to avoid period promotion (see Applicant's specification, paragraph [0005]).

Yoshizawa discloses a computer peripheral device in which mutually different interfaces can be mounted where a CPU is operated on the basis of firmware stored in a nonvolatile memory. Yoshizawa, however, does not teach, disclose or suggest "the plurality of queue heads are directly coupled to the frame list during initialization before coupling any split-isochronous transaction descriptors to the plurality of queue heads where split-isochronous transaction descriptors are supported." Moreover, Yoshizawa does not even mention, at all, the terms: USB host controller, queue heads, frame list, or split-isochronous transaction descriptors.

Wang discloses a USB host controller that includes a batch memory. Wang further discloses that multiple transactions are stored in the batch memory and, using a single interrupt, the USB host controller can execute the batch of transactions. Wang, however, does not teach, disclose or suggest "the plurality of queue heads are directly coupled to the frame list during initialization before coupling any split-isochronous transaction descriptors to the plurality of queue heads where split-isochronous transaction descriptors are supported." That is, Wang uses the basic UHCI data structures and schedule. (See Wang, column 25, lines 16-29).

Neither Yoshizawa, Wang, and therefore, nor the combination of the two teach, disclose or suggest all the limitations of Applicant's amended claims 1 and 8, as listed above, Applicant's amended claims 1 and 8 are not obvious over Yoshizawa in view of Wang since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 1 and

8, namely claims 2-3, and 10-11, respectively, would also not be obvious over Yoshizawa in view of Wang for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 1-4, 6, 8, 10-11 and 13 are respectfully requested.

B. It is asserted in the Office Action that claims 7 and 14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Yoshizawa in view of Wang, and further in view of *NEC Forges Ahead with World's First USB 2.0 Host Controller LSI* ("NEC"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

Applicant's claim 7 indirectly depends on amended claim 1. Applicant has addressed Yoshizawa in view of Wang regarding claim 1 above in section I(A). Applicant's claim 14 directly depends on amended claim 8. Applicant has addressed Yoshizawa in view of Wang regarding claim 8 above in section I(A).

NEC discloses using a typical USB 2.0 host controller. Clearly, NEC does not teach, disclose or suggest "the plurality of queue heads are directly coupled to the frame list during initialization before coupling any split-isochronous transaction descriptors to the plurality of queue heads where split-isochronous transaction descriptors are supported."

Therefore, even if Yoshizawa and Wang were combined with NEC, the resulting invention would still not teach, disclose or suggest all the limitations of Applicant's amended claims 1 and 8, as listed above. Therefore, Applicant's amended claims 1 and 8 are not obvious over Yoshizawa in view of Wang, and further in view of NEC since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 1 and 8, namely claims 7, and 14, respectively, would also not be obvious over Yoshizawa in view of Wang, in further view of NEC for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 7 and 14 are respectfully requested.

C. It is asserted in the Office Action that claim 9 is rejected under 35 U.S.C. §103(a) as being unpatentable over Yoshizawa in view of Wang, and further in view of U.S. Patent No. 6,920,245 issued to Hirayama ("Hirayama"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

Applicant's claim 9 directly depends on amended claim 8. Applicant has addressed Yoshizawa in view of Wang regarding claim 8 above in section I(A).

Hirayama discloses an image processing device for processing a color image read from an original, for example, in an image forming apparatus such as a digital color copying machine for forming a copy image of a color image, and also to an image forming device such as a digital color copying machine using this image processing apparatus. Hirayama does not relate, at all, to USB host controllers. Moreover, Hirayama does not teach, disclose or suggest "the plurality of queue heads are directly coupled to the frame list during initialization before coupling any split-isochronous transaction descriptors to the plurality of queue heads where split-isochronous transaction descriptors are supported."

Therefore, even if Yoshizawa and Wang were combined with Hirayama, the resulting invention would still not teach, disclose or suggest all the limitations of Applicant's amended claim 8, as listed above. Therefore, Applicant's amended claim 8 is not obvious over Yoshizawa in view of Wang, and further in view of Hirayama since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claim that directly depends from amended claim 8, namely claim 9, would also not be obvious over Yoshizawa in view of Wang, in further view of Hirayama for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejection for claim 9 is respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1-4, 7-11 and 14, patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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Dated: January 20, 2006

By: _____

Steven Laut, Reg. No. 47,736

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on January 20, 2006.

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